SEMICONDUCTOR ARRANGEMENT

ABSTRACT OF THE DISCLOSURE

A semiconductor packaging arrangement, or module, includes a printed circuit board having an electrical interconnect thereon and a semiconductor package mounted to the printed circuit board. The semiconductor package includes a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer. The fractional portion of the wafer has a plurality of electrical contacts electrically connected to the chips. The package also includes a dielectric member having an electrical conductor thereon. The electrical conductor are electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips with portions of the electrical conductor spanning the regions in the fractional portion of the wafer. A connector is provided for electrically connecting the electrical conductor of the package to the electrical interconnect of the printed circuit board.